APPLICATION

FOR

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TITLE: LOW LIGHT SENSOR SIGNAL TO NOISE IMPROVEMENT

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LOW LIGHT SENSOR SIGNAL TO NOISE IMPROVEMENT

Cross Reference To Related Applications

This application claims the benefit of U.S. Provisional Application Serial No. 60/093,842, filed on July 22, 1998.

Background

An image sensor can be used in low illumination conditions. It can be necessary to amplify the signal from the sensor used in this way. One typical way of doing this is to "bin" the pixels. For example, a group of four pixels is taken together, and handled as a group. This obtains the signal from all four pixels as an increased-level pixel.

A similar issue can exist when high frame rates are used, where each frame of received signal can be integrated only for a relatively short period of time.

High speed readout produces additional similar issues. Specifically, the high speed readout can be read in bursts. Each of the bursts can be for example a unit, e.g., row or a column, of output of the image sensor. Each unit can be associated with its own unit amplifier to allow the effective unit amplification to be carried out faster. However, unit-to-unit fixed pattern noise can result from mismatched in amplifier voltage offset or gain.

Summary

The present system teaches a device which amplifies according to a combined operation that reduces fixed pattern noise and reduces offsets among the column amplifiers.

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Brief Description of the Drawings

These and other aspects will now be described in detail with reference to the accompanying drawings, wherein:

FIG. 1 shows a first embodiment of a multiple binning

10   system;

FIGs. 2A and 2B show a circuit for amplification and fixed pattern noise rejection;

FIG. 3 shows a timing chart of signals in the FIG 2A/2B circuit; and

15   FIG. 4 shows a dual output stage circuit for adding.

Description of the Embodiments

A disclosed embodiment reads the pixels out in column-parallel mode, wherein an entire row of pixels is read-out at a single time. The pixels can be active pixels that have a

20   photoreceptor, an in-pixel buffer transistor and an in-pixel selection transistor. The signal-to-noise response of this circuitry can be improved by binning the signals from adjacent

units, (here rows) and using the binned result as the output for both rows. This doubles the resulting signal, but adds the noise in quadrature. Hence, the noise only increases by 1.4 while the signal increases by 2.

5   Previous binning operations have reduced the vertical resolution of the sensor by 2.

A disclosed embodiment described herein performs a post-amplification staggered row addition. This produces a number of outputs, each of which has a different output value. The first

10   output 102 corresponds to a sum of row 1 + row 2. The second output corresponds to row 2 + row 3. Adders 101 and 103 are shown for carrying out the addition; however, a single adder could be used.

Hence, each row is used twice, and the same, or almost the

15   same, number of binned signals are obtained as rows. The output signal is still, in general, doubled, while the noise increases only by 1.4. However, this system can have a smaller resolution reduction.

Another embodiment also shown in the left most part of FIG.

20   1 generalizes this approach to the addition of more than two rows. For example, in this second embodiment, row 1 + row 2 + row 3 is added by adder 120, to form a tripled signal 125. Another tripled signal 127 is formed by using adder 122 to add row 2 + row 3 + row 4. In general, n units are added, and each

unit is used n times. However, this trades off image sharpness against noise. This feature effectively carries out a smoothing function and hence can reduce image sharpness.

FIGs. 2A and 2B show an embodiment of an amplifier 199 for noise-reduced column wise gain. The operation is described herein with reference to the timing chart of FIG. 3. This timing chart also shows the separation between the row timing, which is carried out simultaneously for all columns, and the column readout timing, which is carried out one column at a time.

Each pixel output is connected to the pixel out node 200. First, the pixel reset voltage is sampled onto the capacitor C1, by turning on the NMOS transistor M2 using the Sh1_in control signal. The signal voltage is subsequently sampled onto capacitor C2 similarly using the Sh2_in control signal via the transistor M4. An amplification cycle is then initiated, by resetting the amplifier using the phi_reset control signal 210 and phi_reset_bar control signal 212. These turn on the CMOS reset switches M8/M9 thereby shorting across the capacitor C3. At the same time, the NMOS switch M3 is turned on via the control signal Sh1_out 206, thereby feeding the reset level to the gate of PMOS follower M7 and charging the capacitor VC4.

The gain of the signal is set by a variable capacitor variableC4. During the reset phase, the amplifier output settles to the reset voltage Vclamp (V_{CL}) which is applied to the non-

inverting input of the of the op amp 220, plus Vos which represents the offset of the amplifier 220. This voltage level is used to clamp the variable capacitance variable C4. Hence, this voltage is sampled onto capacitor C5 shown in FIG. 2B by

5   turning on the NMOS switch M10. The NMOS switch M10 is controlled by the control signal phi_out_1 302.

The amplifier is then released from reset by allowing phi_reset_bar and phi_reset to go inactive, and by allowing phi_out_1 to go inactive. This begins the amplification phase.

10   First, the pixel signal level is connected to PMOS source follower M7 by making SH1_out inactive to turn off M3, and making SH2_out active to turn on M5. This connects the signal level from pixel out to the PMOS M7 causing its output to slew to a new level. This reduces the charge on one plate of capacitor VC4,

15   pumping the other plate according to form a voltage delta V d⁻ signal-reset. This causes the op amp 220, correspondingly, to settle to a new level. As conventional, the output 222 of the op amp settles to a new level which restores input node B- to its original level (here V_{CL}).

20   The new level at the op amp output 222 corresponds to VCL + Vos + deltaV*(C4/C3). This value is sampled onto capacitor C6 via the NMOS switch M11 controlled by the control signal phi_out_2. The above represents the actions in the rows.

The columns are then processed. The column output is then

sampled using a fixed pattern noise rejection crowbar circuitry.
The crowbar process shorts the plates of capacitors C5 and C6,
providing a voltage shift between the two output nodes, that
corresponds to the difference between voltages on C5 and C6. The
5   sum of the two voltage shifts is carried out by turning on all of
transistors M12, M13 and M14. This cancels the common components
and provides a voltage output equal to deltaV x (C4/C3). All
amplifier and transistor offset voltages are completely removed.
Hence, the fixed pattern noise only results from column-to-column
10   variations in the value of C4/C3. C3 can be sized to e.g. 0.1
pf, to render this variation insignificant.

The integration/reset speed of this circuit is determined by
the gain-bandwidth characteristics (GBW) of the amplifier 220
based on its load. The load can include capacitors C5 or C6
15   depending on the connection. The integration time is
approximately equal to gain over CBW. The gain bandwidth of the
amplifier in the reset phase of the cycle can lower due to the
increased load ≈ C5 + gain*C3. However in reset, the closed loop
gain is 1. Hence, the reset time is 1 + gain to (1/GBW), which
20   can ten times faster. Hence, reset can be done much faster than
sampling.

FIG. 4 shows this same circuit being used for sequential row
addition. The input/amplification stage 199 of FIG. 2A is
connected to the FPN stage 198 of FIG. 2B. A second fixed

-6-

pattern noise rejection circuit 399 is formed in parallel with the first FPN stage 198. Two "and" gates 402, 404 control the selection of the FPN circuits. The first array 198 output is selected using the signal output A. A low value for output A

5   (output_A_bar) selects the second output array 399.

Timing of the signals in FIG. 3 controls whether the gain of the circuit is positive or negative. Amplification can be inverted by reversing the order of closure of switches M3 and M5. For example, if the reset level C1 is connected during the reset

10   phase and the signal level C2 during amplification, then the final output level is Vos + Vclamp + gain*(Signal-Reset). If the order is reversed, however, the final output level becomes Vos + Vclamp + Gain*(Reset-Signal). This reverses the sense of the signal.

15   Controller 304 produces the signals to alternate the order of amplification in each successive row. The result is stored in either of the capacitors C5 or C7 if phi_out is active, or C6/C8 if phi_out_2 is active. While the reset level is never stored, the output level can be stored.

20   For readout, either the top pair of capacitors C5/C6 or the bottom pair of capacitors C7/C8 is shorted using the crowbar scheme described above. The signal circuit in Figure 4 shows two separate crowbars M12-M14 and M19-M21. Thus, the total output voltage shift is (Vos + Vclamp + Gain*(Signal-Reset)$_{(row\ i)}$ - (Vos
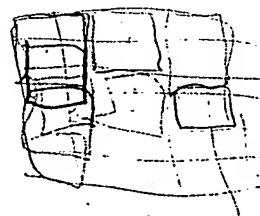
+ Vclamp + Gain*(Reset-Signal)$_{(row\ I+1)}$).   Since the clamp voltage

Vclamp, the offset voltage Vos, and the Gain are the same in both

terns, this reduces to G*(Signal-Reset)$|_{Row}$ i +

(Signal-Reset)$_{|Row\ i+1}$.

5   The amplifier reset level Vos + V_{CL} does not need to be

subtracted from each row independently, since that value is

always from the FIG. 2A circuit and hence is the same each time.

Two independent output stages allow storing the value from one

row for addition to the next row without destroying it during the

10   crowbar readout. This enables each pair of rows to be

sequentially added. For example, rows 1 + 2 can be added in the

pair C5/C6. Rows 2 + 3 can be added in the pair C7/C8. Rows

3 + 4 can be again added in the pair C5/C6.

        Although only a few embodiments have been described in

15   detail above, other embodiments are contemplated by the inventor

and are intended to be encompassed within the following claims.

In addition, other modifications are contemplated and are also

intended to be covered.